REMARKS

Supplemental Information Disclosure Statement

Applicant respectfully brings to the attention of the Examiner the Supplemental Information Disclosure Statement filed by Applicant on October 19, 2004. Note that the Office Action mailed from the PTO on October 18, 2004 crossed in the mail with this Supplemental Information Disclosure Statement.

Objection to the Drawings

The drawings are objected to under 37 CFR 1.83(a), the Office Action stating:

> The drawings are objected to because the structure shown in Fig. 2 is not consistent with the structure recited in claim 1. Specifically, the adder 202 shown in Fig. 2 does not receive the signals recited in the claim. As shown, the adder 202 receives the signals Q180[N:0] from the divide-by-two register 228 at first data inputs A[N:0] and receives the signals GND, Q180[N:1] which is the N-1 most significant signals also from the divide-by-two register at second data inputs B[n:0] whereas the claims recites the adder receives the signals from the first counter circuit.

Applicant has amended Claim 1 to recite that the adder receives the signals from the divide-by-two register. Therefore, the objection is overcome.

Summary of Claim Status

Claims 1-31 are pending in the present application after entry of the present amendment. Claims 1–31 are rejected for the reasons discussed below.

Applicant respectfully acknowledges the statements included in the Office Action that "Claims 1-31 read over the prior art of record..." and "would be allowed if the double patenting rejections and indefiniteness rejections noted herein above are overcome."

Applicant requests the favorable reconsideration of the claims and withdrawal of the pending rejections and objections, in view of the present amendment and in light of the following remarks.

Objections to the Claims

Claims 2-3 are objected to due to certain informalities. Applicant has amended Claims 2 and 3 to correct these informalities as suggested by the Examiner. Therefore, this objection is overcome.

Rejections Under 35 USC 112

Claims 1-13 are rejected as being indefinite under 35 USC 112, the Office Action stating:

> As per Claim 1, the recitation the system (line 1) comprising a first counter circuit (line 5), a divide-by-two register (line 8) is indefinite because it is not consistent with what is described in the specification. In the specification, paragraph 36 describes the divide-by-two register 228 to be part of the first counter circuit 201 (Fig. 2). It means the divide-by-two register 229 is inside the first counter circuit 201, therefore, it does not make sense to recite the system comprises a first counter circuit and a divide-by-two register.

Applicant respectfully traverses this rejection. As is well known, the terms "first circuit" and "second circuit" are used in claims merely to distinguish between two different circuits. A certain group of circuit elements can be referred to as a "first circuit" in one independent claim, and as a "second circuit" in another independent claim. Therefore, one group of circuit elements can certainly be referred to as a "first counter circuit" in the specification, while a different group of circuit elements is referred to as a "first counter circuit" in one or more of the claims.

As the term is used in Claim 1, the term "first counter circuit" does not include the divide-by-two register. For example, in one embodiment described by Claim 1, the "first counter circuit" includes all of the elements included in counter circuit 201 except for divide-by-two register 228 (see Fig. 2).

Applicant respectfully draws the Examiner's attention to MPEP 2173.05(b), which states: "Acceptability of the claim language depends on whether one of ordinary skill in the art would understand what is claimed, in light of the specification." This use of the term "first counter circuit" would be clear to those of ordinary skill in the relevant arts from the fact that the divide-by-two register is included as a separate element in the claim. Further, the Examiner was clearly able to interpret the term correctly while

comparing Claim 1 with Fig. 2, to produce the Objection to the Drawings quoted above.

Therefore, Applicant believes that no correction is necessary.

With regard to Claim 1, the Office Action further states:

> The recitation that [the] clock terminal [is] coupled to the input clock terminal on lines 10-11 appears misdescriptive. As shown in Fig. 2, the clock terminal CK of the divide-by-two register 228 receives the clock update signal CLK_UPDT from the first counter circuit.

Applicant has amended Claim 1 to clarify that the clock terminal of the divide-by-two register is "coupled to receive a clock update signal from the first counter circuit". Therefore, this rejection is overcome.

Claims 2-13 are objected to as being dependent from Claim 1. Therefore, Claims 2-13 are also allowable over the 35 USC 112 rejection.

Rejections for Double-Patenting

Claims 1 and 14-31 are provisionally rejected under the judicially created doctrine of double patenting over co-pending U.S. Patent Application Serial No. 10/651,811. (Note that the present application claims priority to this co-pending application.) In response, Applicant has enclosed herewith a terminal disclaimer for the present invention with respect to the cited application.

Conclusion

No new matter has been introduced by any of the above amendments. All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested. If any action other than allowance is contemplated by the

Examiner, the Examiner is respectfully requested to telephone Applicant's agent, Lois D. Cartier, at 720-652-3733.

Respectfully submitted,

Lois D. Cartier
Agent for Applicant
Reg. No. 40,941

I hereby certify that this correspondence is being deposited with the United States Postal Service as **first class mail** in an envelope addressed to: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450, on November 9, 2004

Pat Slaback
Name

Signature